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L1	1521	703/2.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/11 16:58
L3	955	database and (logic near design)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/11 16:59
L4	564	L3 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/11 17:44
L5	30	("5187668" "5212650" "5313615" "5432707" "5452226" "5487018" "5519627" "5541849" "5623417" "5666288" "5696693" "5699265" "5726902" "5727187" "5757657" "5761664" "5764534" "5818729" "5841663" "5864487" "5956497" "5960184" "6026228" "6080201" "6145117" "6154874" "6216258" "6263483" "6289489" "6308309").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/10/11 17:42
L6	227	hdl and (parameter\$7 near design)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/11 17:43
L7	133	L6 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/11 17:44
L8	75	L7 and database	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2005/10/11 17:44



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Parameterized system design

TD Givargis, F Vahid - HARDWARE SOFTWARE CODESIGN PROC INT WORKSHOP, 2000 - doi.ieeecomputersociety.org

... generics, but rather may require new **HDL** code to ... appears as part of the **SOC design**, such as ... Each configuration of a **parameterized** SOC architecture represents a ...

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Parameterized IP core design

Z Junchao, C Weiliang, W Shaojun - Proc. of 4th Int'l Conf. on ASIC, 2001 - ieeexplore.ieee.org

... 2. **Design** Style At the **HDL** level, there are two ... instance commodity-style IP core or a **parameterized**-style IP ... of IP is an important issue in hardware **design**. ...

Cited by 3 - [Web Search](#) - [ieeexplore.ieee.org](#)

System-Level Exploration for Pareto-Optimal Configurations in Parameterized Systems-on-a-Chip

T Givargis, F Vahid, J Henkel - IEEE ACM INT CONF COMPUT AIDED DES DIG TECH PAP. pp. 25-30. ..., 2001 - doi.ieeecomputersociety.org

... algorithm fits in an **SOC design** flow as follows. As depicted in Figure 1, the **SOC** provider provides a **parameterized** architecture in **HDL** or configurable IC ...

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Increasing Design Quality and Engineering Productivity through Design Reuse

EF Girczyc, S Carlson - DAC, 1993 - portal.acm.org

... be **parameterized** without increasing **design** cost if the description is written in a form that ties functionality to an operating mode parameter at the **HDL** level ...

Cited by 37 - [Web Search](#) - [portal.acm.org](#)

HDL generation from parameterized schematic design system

A Mathur, P Parikh, A Mujumdar, R Shur, T Bulgerin ... - ASIC Conference and Exhibit, 1997. Proceedings., Tenth ..., 1997 - ieeexplore.ieee.org

... **HDL** generation from **parameterized** schematic **design** system Mathur, A. Parikh, P. Mujumdar, A. Shur, R. Bulgerin, T. Mahmood, M. Desai, S. Juneja, P. Alta Group ...

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A Top-Down Mixed-Signal Design Methodology Using a Mixed-Signal Simulator and Analog HDL

T Murayama, Y Gendai - Proceedings of the conference on European **design** automation, 1996 - doi.ieeeecs.org

... LY con-vert,ers, etc) have been **parameterized** for easy ... of the EURO-DAC '96 European **Design** Automation Conference ... and that of verilog-**HDL** was about 1,500 lines ...

[Web Search](#) - doi.ieeecomputersociety.org - [portal.acm.org](#) - [sigda.org](#) - [all 7 versions](#) »

Reusable Internal Hardware Templates

K Agun, JM Chang - IPPS/SPDP Workshops, 1999 - iit.edu

... hardware templates are generic and **parameterized** hardware functions. Internal Hardware Templates The base hardware **design** will be compiled by **HDL** tools, but ...

[View as HTML](#) - [Web Search](#) - [portal.acm.org](#)

The Evolution of Schematic Entry: Moving from Gates to Geography

TH Scott, PL Solutions, O Inc, OR Beaverton - ... Communications Technology Producing Quality Products Mobile ..., 1995 - ieeexplore.ieee.org

... You can now compound all the relevant **design** documents in one place [2]. If the **design** object is a **parameterized** module of **HDL**, you may want to Link the **design** ...


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John Colter, Netscape Navigator

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[CITATION] **The Case for Expressive Systems**

R Pawson, JL Bravard, L Cameron - Sloan Management Review, 1995

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[BOOK] **Architecture and its interpretation: a study of expressive systems in architecture**

JP Bonta - 1979 - New York: Rizzoli

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B Laurel - Reading, MA, 1991 - portal.acm.org

... Richard Pawson, Robert Matthews, Naked objects: a technique for designing more **expressive systems**, ACM SIGPLAN Notices, v.36 n.12, December 2001. ...

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D Ingalls, T Kaehler, J Maloney, S Wallace, A Kay - ACM SIGPLAN Notices, 1997 - portal.acm.org

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Login. Search: The ACM Digital Library The Guide. ...

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A Cookbook for Using the Model-View-Controller User Interface Paradigm in Smalltalk-80

GE Krasner, ST Pope - Journal of Object-Oriented Programming, 1988 - portal.acm.org

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M Van Harmelen - 2001 - portal.acm.org

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- ☐ 1. **On the fundamental design gap in terabit per second packet switching**
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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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the promises of hardware synthesis is providing **logic designers** with little or no experience in ASIC design

image processing, text searching, some **database** queries, some graphics applications, and DNA

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can be factored out in the first step. PSM F-**logic design** step step impl. SQL3 ODMG-93 ?Figure 1:

Modelling Based Design of Object-oriented **Databases** Gyorgy Kov'acs Dept. of Information Systems

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in support of semantic integration of deductive **databases** is proposed. The language allows one to

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compared to other aspect of VLSI design such as **logic design**, simulation, placement, wiring and physical

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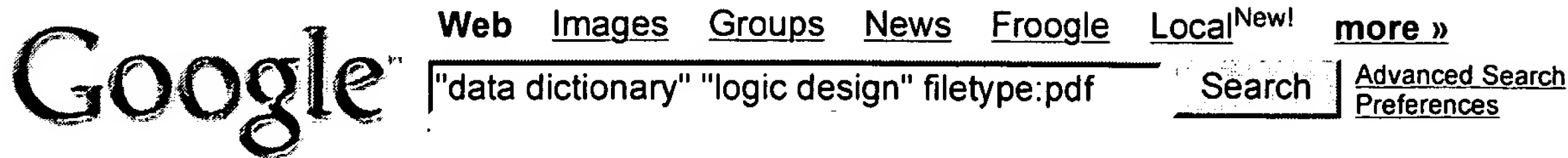
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logic started to gain interest in many areas: **logic design**, switching theory, programming languages,
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